MITSUBISHI ELECTRIC

TENTATIVE

< DIPIPM >

Super mini Full SiC DIPIPM APPLICATION NOTE PSF15S92F6-A

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This application note is supplementary material to explain special features and characteristics of Super mini Full SiC DIPIPMs. When to apply Super mini Full SiC DIPIPMs, please also refer to Super mini DIPIPM Ver.6 series application note in addition.

CHAPTER 1 INTRODUCTION

1.1 Features of Super mini Full SiC DIPIPM

Super Mini Full SiC DIPIPM (hereinafter called Full SiC DIP) is an ultra-small compact transfer molded intelligent power module integrating SiC MOSFET chip which is the next generation high efficiency power chips. Power chips, drive and protection circuits are integrated in the module with transfer molding resin.

Full SiC DIP can improve inverter efficiency drastically by embedding SiC MOSFET chips, and additionally the Full SiC DIP takes over conventional Super mini DIPIPM Ver.6 series (such as incorporating bootstrap diode with resistor, LVIC temperature analog signal output and its de facto standard package for household electric appliances). This compatibility enables to divert the conventional inverter board easily (though partly changes required) and to expand the lineup of installed systems.

Main features of Full SiC DIP are as below.

- ***Newly developed SiC MOSFET are integrated for improving efficiency.***
- ***Current rating lineup of 15A/600V product***
- ***NO requirement of negative bias by mounting MOSFET with high threshold voltage V_{GSth}.***
- ***Single DC 18V power supply drive with bootstrapping scheme.***
- ***Safety operating SiC MOSFET by protection functions.***
- ***Easy to replace from conventional Ver.6 due to pin and function compatibility.***

About detailed differences, please refer Section 1.5. Fig.1-1-1, Fig.1-1-2 and Fig.1-1-3 show the outline, internal cross-section structure and loss simulation results (Typical) respectively.

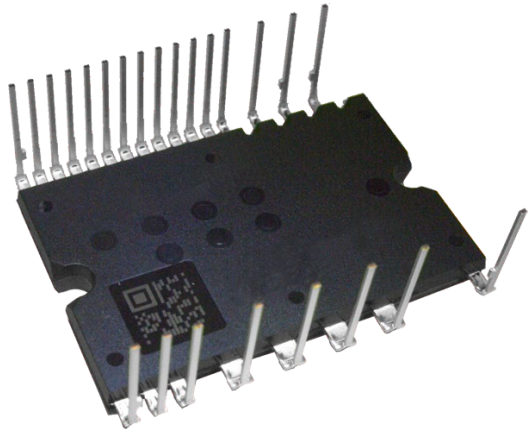


Fig.1-1-1 Package photograph

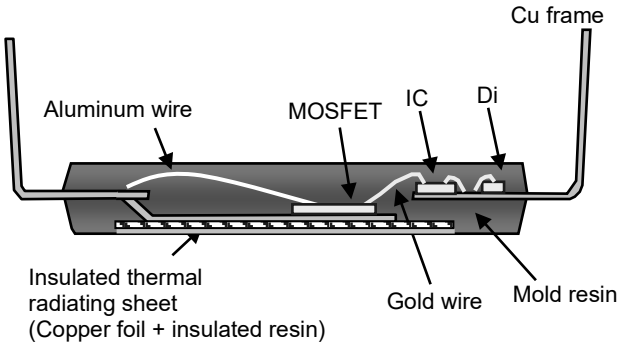
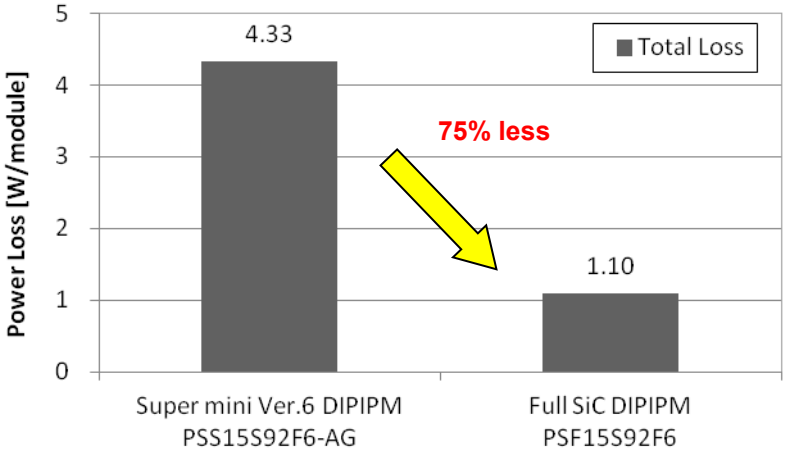


Fig.1-1-2 Internal cross-section structure



[Common calculation condition]
Simulation model: 3 phase PWM
Vcc=V_{DD}=300V, M=1, P.F=0.8, **Io=1Arms**, **fc=5kHz**, fo=60Hz, T_j=T_{ch}=125°C

[Calculation condition for PSS15S92F6-AG]
V_D=V_{DB}=15V, V_{CE}=Typ., V_{EC}=Typ.,
Switching loss=Typ.

[Calculation condition for PSF15S92F6-A]
V_D=V_{DB}=18V, $V_{DS(on)}$=Typ., $V_{SD(on)}$=Typ.,
Switching loss=Typ.

Fig.1-1-3 Loss simulation results (Typical)

1.2 Functions

Full SiC DIP has following functions and inner block diagram as described in Fig.1-2-1.

- For P-side MOSFETs:
  - Drive circuit, High voltage level shift circuit;
  - Control supply under voltage (UV) lockout circuit (without fault signal output).
  - Built-in bootstrap diode (BSD) with current limiting resistor
- For N-side MOSFETs:
  -Drive circuit;
  -Short circuit (SC) protection circuit (by inserting external shunt resistor into main current path)
  -Control supply under voltage (UV) lockout circuit (with fault signal output)
  -Outputting LVIC temperature by analog signal
- Fault Signal Output
  -Corresponding to N-side MOSFET SC and N-side UV
- MOSFET Drive Supply
  -Single **DC18V** power supply (in the case of using bootstrap method)
- Control Input Interface
  -Schmitt-triggered 3V, 5V input compatible, high active logic.
- UL recognized
  -UL 1557 File E323585

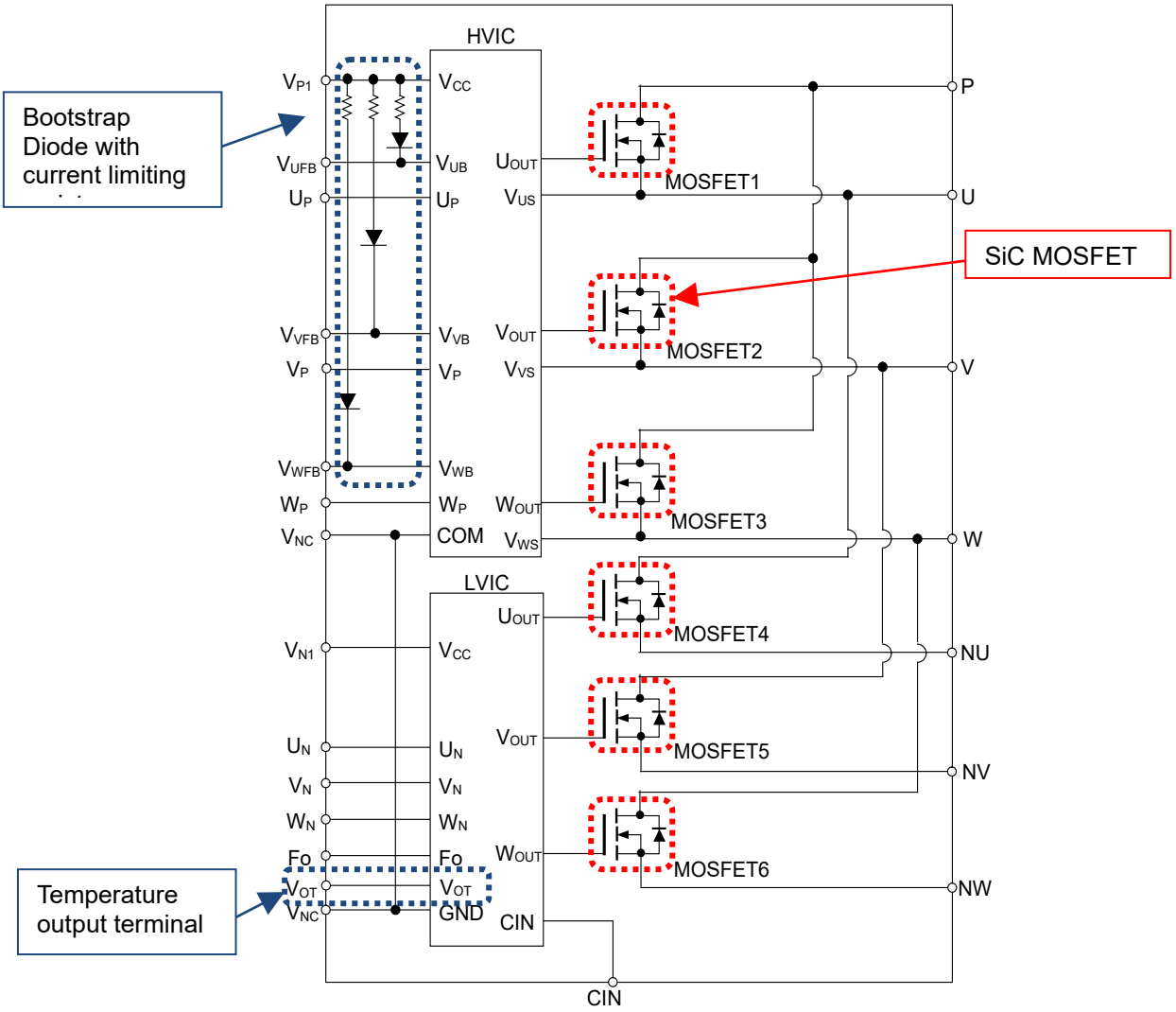


Fig.1-2-1 Inner block diagram

1.3 Target Applications

Motor drives for household electric appliances, such as air conditioners, washing machines, refrigerators
Low power industrial motor drive except automotive applications

1.4 Product Line-up

The lineup of Super mini Full SiC DIPIPM series is described in Table 1-4-1.

Table 1-4-1 Full SiC DIP Line-up with temperature output function

Type Name	MOSFET Rating	Motor Rating [1)]	Isolation voltage Viso
PSF15S92F6-A	15A/600V	1.5kW / 220VAC	V_{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)

(1) The motor rating is based on generally applicable motor capacity in industrial general-purpose inverters. The applicable motor capacity may vary depending on its usage conditions.

1.5 The Differences between Previous Series and This Series

Following tables show main differences between Super mini Full SiC DIPIPM (Full SiC DIP, PSF15S92F6-A) and Super mini DIPIPM Ver.6 (DIP Ver.6, PSS**S92*6-AG). For more information, please refer each datasheet.

Table 1-5-1 Differences of functions and outlines

Items	PSS**S92*6-AG Super mini DIPIPM Ver.6	PSF15S92F6-A Super mini Full SiC DIPIPM
P-side control supply volatge V_{DB} [1)]	Typ. 15V (13V~18.5V)	**Typ. 18V** (15V~22V)
N-side control supply voltage V_D [1)]	Typ. 15V (13.5V~16.5V)	**Typ. 18V** (17V~19V)
Built-in bootstrap diodes	Built-in with current limiting resistor	←
Temperature protection [2)]	OT or VOT	VOT
N-side IGBT emitter terminal	Open	←
Terminal Shape	Long	←

(1) For conventional DIPIPM series such as DIP Ver.6, P-side and N-side control supply voltage V_{DB} and V_D are 15V typical. On the other hand, Full SiC DIP requires typical 18V power supply drive for V_{DB} and V_D. This higher V_{DB} and V_D enables Full SiC DIP to have enough current carrying capacity.
(2) Temperature protection function of Full SiC DIP is VOT function only.

Table 1-5-2 Differences of control (protection) part specifications (15A/600V)

Items	Symbol	PSS**S92*6-AG Super mini DIPIPM Ver.6	PSF15S92F6-A Super mini Full SiC DIPIPM
Circuit current for P-side driving	I_D	Max 2.80mA	Max 3.50mA
Circuit current for P-side driving	I_{DB}	Max. 0.10mA	Max. 0.38mA
Trip voltage for P-side control supply under voltage protection	UV_{DBt}	Min. 7.0V	Min. 10.0V
Reset voltage for P-side control supply under voltage protection	UV_{DBr}	Min. 7.0V	Min. 10.5V
Bootstrap Di forward voltage	V_F	Typ. 1.7V @10mA	Typ. 1.3V @10mA

Table 1-5-2 Differences of main electric characteristics and recommended operating conditions
(15A/600V, Tch = 25°C, unless otherwise noted)

Items	Symbol	PSS15S92*6-AG	PSF15S92F6-A
		Super mini DIPIPM Ver.6	Super mini Full SiC DIPIPM
Collector-emitter saturation voltage Drain-source on-state voltage	V_{CEsat} $V_{DS(on)}$	Typ. 1.70V @15A Typ. 0.90V @1.5A	Typ. 1.10V @15A Typ. 0.10V @1.5A
FWDi forward voltage Source- drain voltage	V_{EC} $V_{SD(off)}$	Typ. 2.50V @15A	Typ. 4.00V@15A [3)]
Allowable r.m.s. current	Io	7.5Arms @f_{PWM}=5kHz 4.5Arms @f_{PWM}=15kHz	10Arms @f_{PWM}=5kHz 8Arms @f_{PWM}=15kHz

(3) Source-drain voltage means V_F of body diode when there is no ON signal at the free wheeling operation phase. When the MOSFET turning on during the free wheeling phase (i.e. complementary switching state), the channel of the MOSFET conducts by the ON signal and its current path is enlarged by the body diode portion and the MOSFET channel portion. So the conduction loss is greatly reduced compared with the case of only the body diode.

For more detail and the other characteristics, please refer the datasheet for each product.

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

This chapter describes specifications, short circuit protection function and its sequence of Super mini Full SiC DIPIPM. For its packages (e.g. outline drawing, marking and terminal arrangement) and its mounting method (e.g. insulation distance, tightening procedure and soldering condition), please refer to Super mini DIPIPM Ver.6 series application note.

2.1 Super Mini Full SiC DIPIPM Specifications

Full SiC DIP specifications are described below by using PSF15S92F6-A(15A/600V) as representative example. Please also refer to its datasheets for the detailed description. For its Mechanical Characteristics and Ratings, please refer to Super mini DIPIPM Ver.6 series application note.

2.1.1 Maximum Ratings

The maximum ratings of PSF15S92F6-A(15A/600V) are shown in Table 2-1-1.

Table 2-1-1 Maximum Ratings

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{DD}	Supply voltage	Applied between P-NU,NV,NW	450	V	(1)
$V_{DD(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V	(2)
V_{DSS}	Drain-source voltage		600	V	(3)
$\pm I_D$	Each MOSFET drain current	T_{ch}= 25°C (Note 1)	15	A	(4)
$\pm I_{DP}$	Each MOSFET drain current (peak)	T_{ch}= 25°C, less than 1ms	30	A	
T_{ch}	Channel temperature	(Note 2)	-30~+150	°C	(5)

Note1: Pulse width and period are limited due to channel temperature.
Note2: The maximum channel temperature rating of built-in power chips is 150°C (@Tc≤100°C). However, to ensure safe operation of DIPIPM, the average channel temperature should be limited to Tch(Ave)≤125°C (@Tc≤100°C).

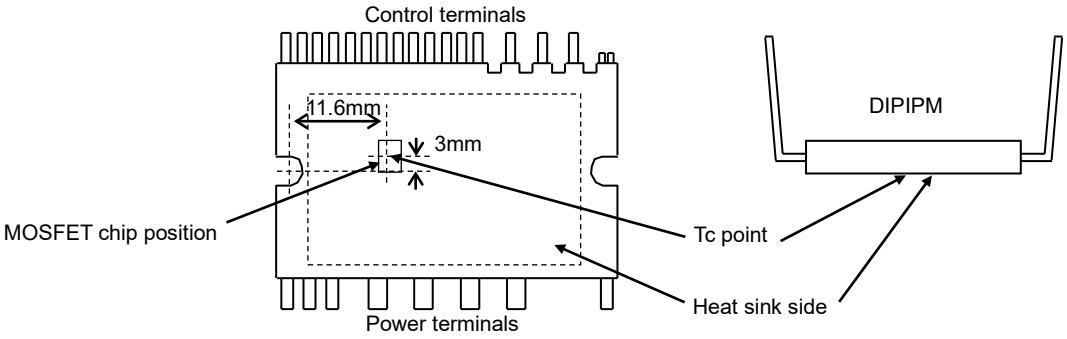
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	24	V_D
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	24	V_{DB}
V_{IN}	Input voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V_{IN}
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V_{FO}
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 17~19V, Inverter Part T_{ch}= 125°C, non-repetitive, less than 2μs	400	V	(6)
T_C	Module case operation temperature	Measurement point of Tc is provided in the below Fig.	-30~+100	°C	
T_{stg}	Storage temperature		-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}	(7)

Fig. Tc measurement position (8)



[Explanation of each item]

(1)	V_{DD}	The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.
(2)	$V_{DD(surge)}$	The maximum P-N surge voltage in switching state. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge under this voltage.
(3)	V_{DSS}	The maximum sustained drain-source voltage of built-in MOSFET.
(4)	$\pm I_D$	The allowable current flowing into drain electrode (@Tc=25°C). Pulse width and period are limited due to the channel temperature T_{ch}.
(5)	T_{ch}	The maximum channel temperature rating is 150°C. But for safe operation, it is recommended to limit the average channel temperature up to 125°C. Repetitive temperature variation ΔT_{ch} affects the life time of power cycle, so refer life time curves for safety design.
(6)	$V_{DD(PROT)}$	The maximum supply voltage for turning off MOSFET safely in the case of an SC or OC fault. The power chip might be damaged if supply voltage exceeds this specification.
(7)	Isolation voltage	Isolation voltage of Super mini DIPIPM is the voltage between all shorted pins and copper surface of DIPIPM. The maximum rating of isolation voltage of Super mini DIPIPM is 1500Vrms. But if such as convex shape heat radiation fin will be used for enlarging clearance between outer terminals and heat radiation fin (2.5mm or more is recommended), it is able to correspond isolation voltage 2500Vrms. Super mini DIPIPM is recognized by UL at the condition 2500Vrms with convex shape heat radiation fin.
(8)	Tc measurement position	Tc (case temperature) is defined to be the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

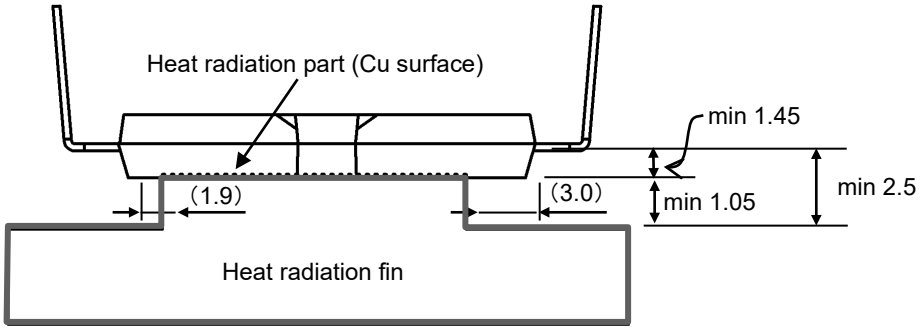


Fig.2-1-1 In the case of using convex fin (unit: mm)

[Power chip position]
Fig.2-1-2 indicates the position of the each power chips. (This figure is the view from laser marked side.)

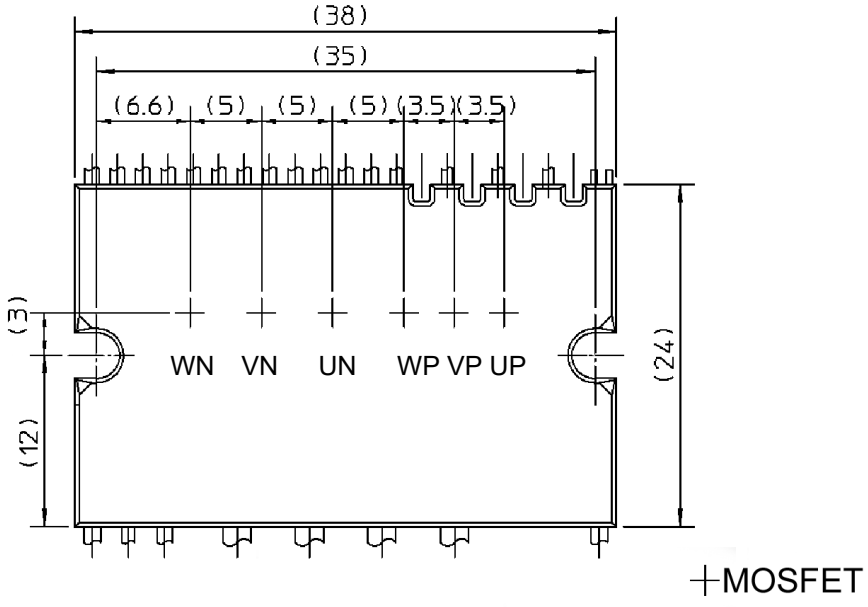


Fig.2-1-2 Power chip position (Dimension in mm)

2.1.2 Thermal Resistance

Table 2-1-2 shows the thermal resistance of PSF15S92F6-A(15A/600V).

Table 2-1-2 Thermal resistance of PSF15S92F6-A(15A/600V)

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(ch-c)Q}$	Channel to case thermal resistance (Note 3)	Inverter MOSFET part (per 1/6 module)	-	-	3.7	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•K).

The above data shows the thermal resistance between chip channel and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-3. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max)
For example, the MOSFET transient thermal impedance of PSF15S92F6-A in 0.3s is 3.7×0.8=3.0K/W.
The transient thermal impedance isn't used for constantly current, but for short period current (ms order).
(E.g. In the cases at motor starting, at motor lock・・・)

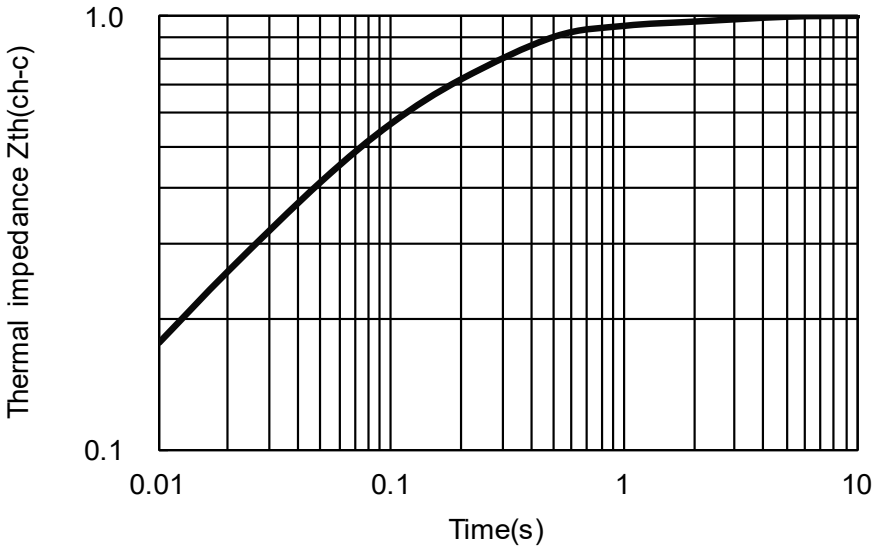


Fig.2-1-3 Typical transient thermal impedance

2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics of PSF15S92F6-A(15A/600V).

Table 2-1-3 Static characteristics and switching characteristics of PSF15S92F6-A(15A/600V)

INVERTER PART (Tch = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{DS(on)}$	Drain-source on-state voltage	V_D=V_{DB} = 18V, V_{IN}= 5V	I_D = 15A, T_{ch} = 25°C	-	1.10	1.80	V
			I_D = 15A, T_{ch} = 125°C	-	1.10	1.80	
			I_D =1.5A, T_{ch} = 25°C	-	0.10	0.25	
$V_{SD(off)}$	Source- drain voltage	V_D=V_{DB} = 18V,V_{IN}= 0V, -I_D= 15A		-	4.00	5.00	V
t_{on}	Switching times	V_{DD}= 300V, V_D= V_{DB}= 18V I_D= 15A, T_{ch}= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		0.70	1.30	1.85	μs
$t_{c(on)}$				-	0.10	0.36	μs
t_{off}				-	1.50	2.10	μs
$t_{c(off)}$				-	0.10	0.18	μs
t_{rr}				-	0.10	-	μs
I_{DSS}	Drain-Source cut-off current	V_{DS}=V_{DSS}	T_{ch} = 25°C	-	-	1	mA
			T_{ch} =125°C	-	-	10	

Switching time definition and performance test method are shown in Fig.2-1-4 and 2-1-5.
Switching characteristics are measured by half bridge circuit with inductance load.

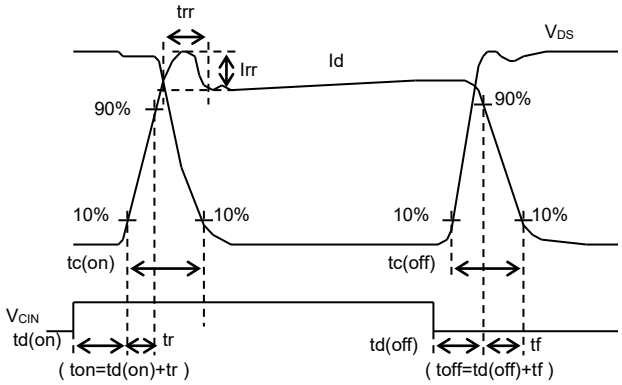


Fig.2-1-4 Switching time definition

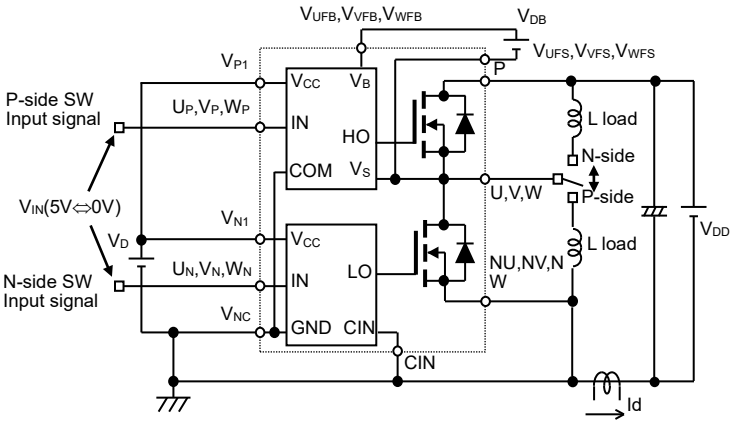


Fig.2-1-5 Evaluation circuit (inductive load)

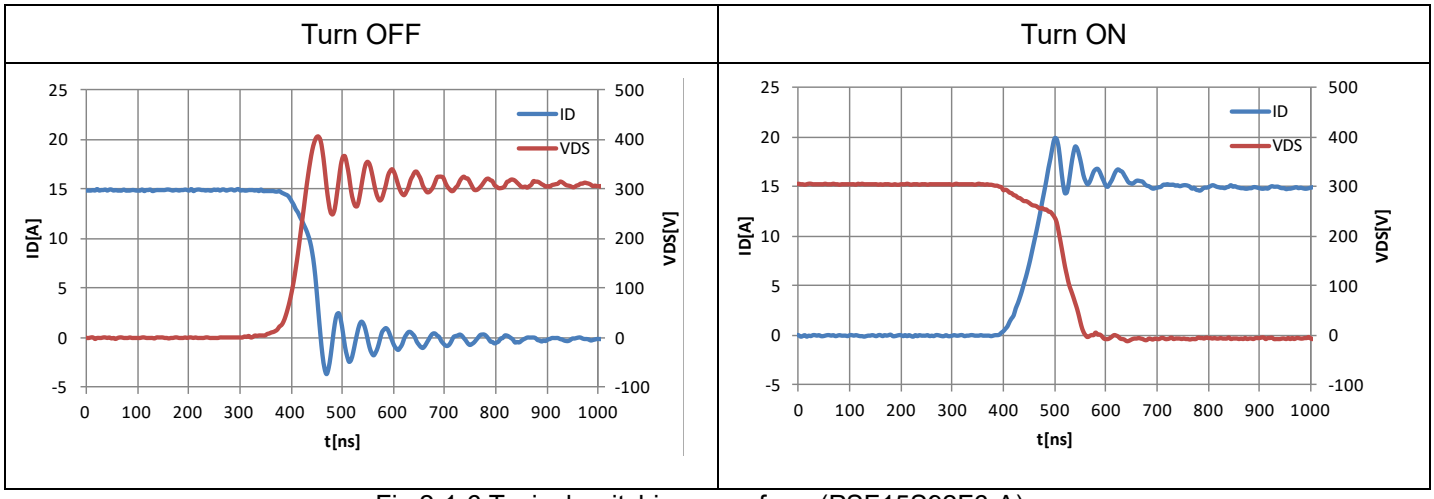


Fig.2-1-6 Typical switching waveform (PSF15S92F6-A)
Conditions: V_{DD}=300V, V_D=V_{DB}=18V, I_D=15A, T_{ch}=25°C, Inductive load half-bridge circuit

Table 2-1-4 shows the typical control part characteristics of PSF15S92F6-A(15A/600V).

Table 2-1-4 Control (Protection) characteristics of PSF15S92F6-A(15A/600V)

CONTROL (PROTECTION) PART (Tch = 25°C, unless otherwise noted)*

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=18V, V_{IN}=0V	-	-	3.50	mA
			V_D=18V, V_{IN}=5V	-	-	3.50	
I_{DB}		Each part of V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	V_D=V_{DB}=18V, V_{IN}=0V	-	-	0.38	
			V_D=V_{DB}=18V, V_{IN}=5V	-	-	0.38	
$V_{SC(ref)}$	Short circuit trip level	V_D = 18V (Note 4)		0.455	0.480	0.505	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	T_{ch} ≤125°C	Trip level	10.0	-	12.0	V
UV_{DBr}			Reset level	10.5	-	12.5	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature output	Pull down R=5.1kΩ (Note 5)	LVIC Temperature=90°C	2.63	2.77	2.91	V
			LVIC Temperature=25°C	0.88	1.13	1.39	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	(Note 6)		20	-	-	μs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	2.10	2.60	V
$V_{th(off)}$	OFF threshold voltage			0.80	1.50	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.35	0.65	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor		0.9	1.3	1.7	V
R	Built-in limiting resistance	Included in bootstrap Di		48	60	72	Ω

Note 4 : SC protection works only for N-side MOSFETs. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5 : DIPIPM don't shutdown MOSFETs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM.

6 : Fault signal Fo outputs when SC or UV protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20μs), but at UV failure, Fo outputs continuously until recovering from UV state. (But minimum Fo pulse width is 20μs.)

Recommended operating conditions of PSF15S92F6-A(15A/600V) are given in Table 2-1-5.
Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

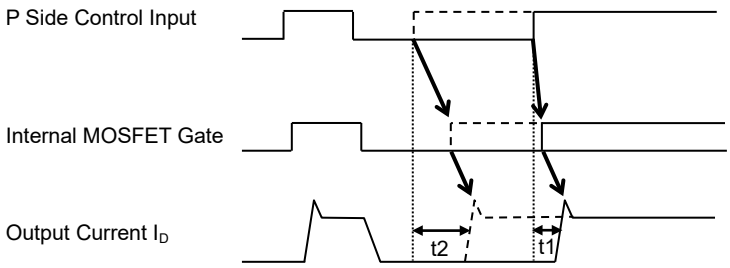
Table 2-1-5 Recommended operating conditions of PSF15S92F6-A(15A/600V)

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage	Applied between P-NU, NV, NW		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		17.0	18.0	19.0	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		15.0	18.0	22.0	V
ΔV_D, ΔV_{DB}	Control supply variation			-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal		1.5	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 100°C$, $T_{ch} \leq 125°C$		-	5	20	kHz
I_O	Allowable r.m.s. current	V_{DD} = 300V, V_D = V_{DB}=18V, P.F = 0.8, Sinusoidal PWM $T_C \leq 100°C$, $T_{ch} \leq 125°C$ (Note7)	f_{PWM}= 5kHz	-	-	10.0	Arms
			f_{PWM}= 15kHz	-	-	8.0	
PWIN(on)	Minimum input pulse width	(Note 8)		0.7	-	-	μs
PWIN(off)		200V≤V_{DD}≤350V, 17V≤V_D≤19V, 15V≤V_{DB}≤22V, -30°C≤Tc≤100°C, N-line wiring inductance less than 10nH (Note 9)	Between rated current and 1.7 times of rated current	1.5	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)		-5.0	-	+5.0	V
Tch	Channel temperature			-20	-	+125	°C

Note 7: Allowable r.m.s. current depends on the actual application conditions.
8: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).
9: IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off). Please refer below about delayed response.

Delayed Response against Shorter Input Off Signal than PWIN(off) (P-side only)



Real line: off pulse width > PWIN(off); turn on time t1
Broken line: off pulse width < PWIN(off); turn on time t2
(t1:Normal switching time)

About Control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

2.2 Protective Functions and Operating Sequence

Full SiC DIP has Short circuit (SC), Under Voltage of control supply (UV) and temperature output (V_{OT}) for protection function. For SC and UV functions, the operating principle and sequence are described below. For V_{OT} function, please refer to Super mini DIPIPM Ver.6 series application note.

2.2.1 Short Circuit Protection

1. General

Full SiC DIP uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection Vsc(ref) is typ. 0.48V.

In case of SC protection happens, all the gates of N-side three phase MOSFETs will be interrupted together with a fault signal output. To prevent DIPIPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: 1.5μ ~ 2μs) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.

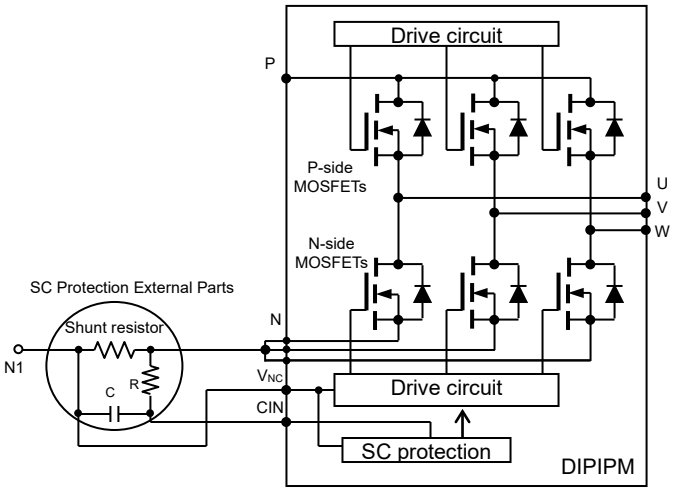


Fig.2-2-1 SC protecting circuit

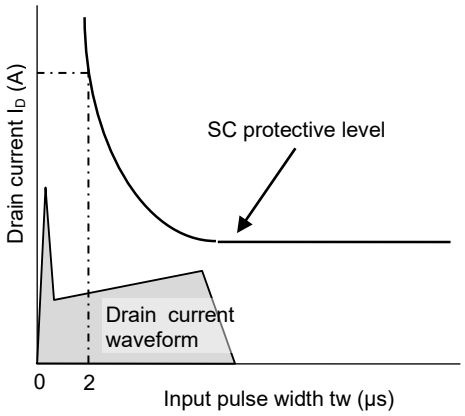


Fig.2-2-2 Filter time constant setting

2. SC protection Sequence

SC protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: MOSFET ON and carrying current.
a2. Short circuit current detection (SC trigger).
(It is recommended to set RC time constant 1.5~2.0μs so that MOSFET shut down within 2.0μs when SC.)
a3. All N-side MOSFETs gate are hard interrupted.
a4. All N-side MOSFETs turn OFF.
a5. Fo outputs for t_{Fo}=minimum 20μs.
a6. Input = “L”. MOSFET OFF
a7. Fo finishes output, but MOSFETs don't turn on until inputting next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: MOSFET ON and outputs current.

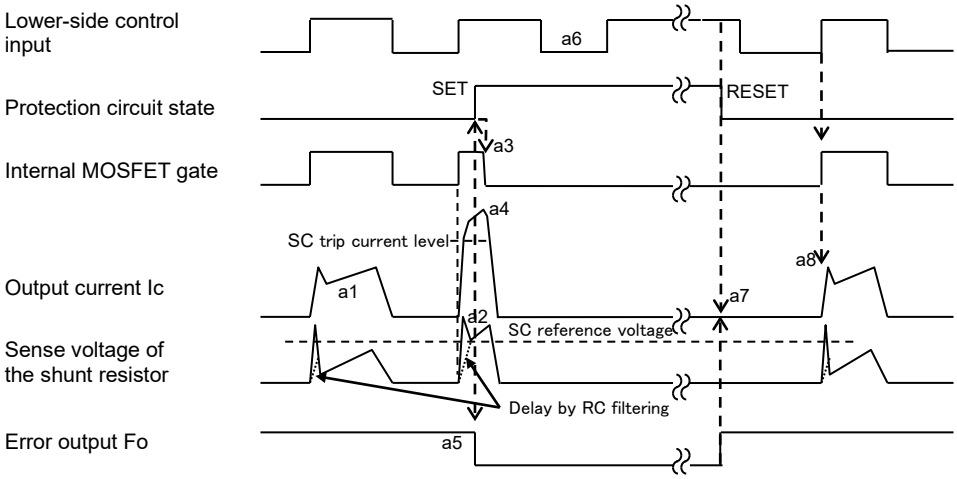


Fig.2-2-3 SC protection timing chart

3. Determination of Shunt Resistance

(1) Shunt resistance

The value of current sensing resistance is calculated by the following expression:
$R_{Shunt} = V_{SC(ref)} / SC$
where $V_{SC(ref)}$ is the referenced SC trip voltage.

The maximum SC trip level SC(max) should be set less than the MOSFET minimum saturation current which is 1.7 times as large as the rated current. For example, the SC(max) of PSF15S92F6-A should be set to 15x1.7=25.5A. The parameters ($V_{SC(ref)}$, R_{Shunt}) tolerance should be considered when designing the SC trip level.

For example of PSF15S92F6-A, there is +/-0.025V tolerance in the spec of $V_{SC(ref)}$ as shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$

Condition	Min.	Typ.	Max.	Unit
at Tch=25°C, V_D=15V	0.455	0.480	0.505	V

Then, the range of SC trip level can be calculated by the following expressions:

$R_{Shunt(min)}=V_{SC(ref)\ max} /SC(max)$
$R_{Shunt(typ)}= R_{Shunt(min)} / 0.95^*$ then $SC(typ) = V_{SC(ref)\ typ} / R_{Shunt(typ)}$
$R_{Shunt(max)}= R_{Shunt(typ)} \times 1.05^*$ then $SC(min)= V_{SC(ref)\ min} / R_{Shunt(max)}$
*)This is the case that shunt resistance tolerance is within +/-5%.

So the SC trip level range is described as Table 2-2-2.

Table 2-2-2 Operative SC Range (R_{Shunt}=19.8mΩ (min), 20.8mΩ (typ), 21.8mΩ(max)

Condition	Min.	Typ.	Max.	Unit
at Tch=25°C	20.9	23.1	25.5	A

(e.g. 19.8mΩ ($R_{shunt(min)}$)= 0.505V (=$V_{SC(max)}$) / 25.5A(=SC(max))

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

(2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIPIPM.
When the voltage drop on the external shunt resistor exceeds the SC trip level, the time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$

$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

Vsc : the CIN terminal input voltage, Ic : the peak current, τ : the RC time constant

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to MOSFET gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	Min.	Typ.	Max.	Unit
IC transfer delay time	-	-	0.6	μs

Therefore, the total delay time from an SC level current happened to the MOSFET gate shutdown becomes:

t_{TOTAL}=t1+t2

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4.
Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.
In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-2-4 DIPIPM operating behavior versus control supply voltage

Control supply voltage(V_D, V_{DB})	Operating behavior
0 – 4.0V (both P and N-side)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally MOSFET does not work. But external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4.0 – UV_{Dt} (N-side) 4.0 – UV_{DBt} (P-side)	**Within the operating range of UV function** UV function becomes active and output Fo (N-side only). Even if control signals are applied, MOSFET does not work.
UV_{Dt} – 17.0V(N-side) UV_{DBt} – 15.0V (P-side)	MOSFET can work, however, at this state its conducting loss and its switching loss will increase than its specification values, and result extra channel temperature rise.
17.0 – 19.0V (N-side) 15.0 – 22.0V (P-side)	**Recommended conditions** MOSFET works normally.
19.0 – 24.0V (N-side) 22.0 – 24.0V (P-side)	MOSFET works, however, at this state its switching speed becomes faster and its saturation current becomes larger than specification values, and increasing SC broken risk.
24.0V – (both P and N-side)	The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

Recommendation of more stable Control Supply

When divert the conventional inverter board, please note that recommended condition of control power supply voltage are changed. For high frequency operation, control supply voltage will easily fluctuate and the above influences may appear conspicuously.
For Full SiC DIP, more stable control supply is highly recommended than the conventional DIPIPMs. Please verify the actual system enough whether the supply voltage can be stably supplied within the recommended range.

[N-side UV Protection Sequence]

a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but MOSFET turns ON by next ON signal (L→H). MOSFET of each phase can return to normal state by inputting ON signal to each phase.
a2. Normal operation: MOSFET ON and carrying current.
a3. V_D level dips to under voltage trip level. (UV_{Dt}).
a4. All N-side MOSFETs turn OFF in spite of control input condition.
a5. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during V_D keeps below UV_{Dr}.
a6. V_D level reaches UV_{Dr}.
a7. Normal operation: MOSFET ON and outputs current.

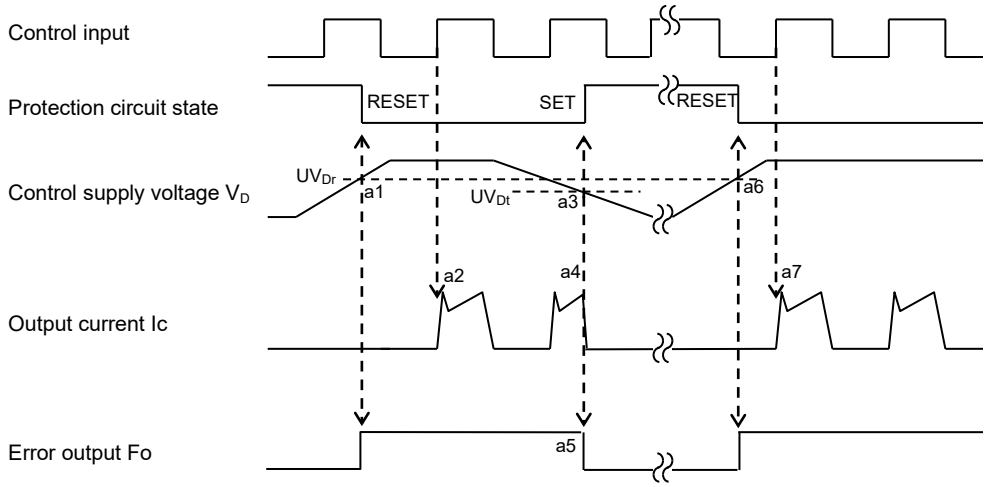


Fig.2-2-4 Timing chart of N-side UV protection

[P-side UV Protection Sequence]

a1. Control supply voltage rises: After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied (L→H).
a2. Normal operation : MOSFET ON and carrying current.
a3. V_{DB} level dips to under voltage trip level (UV_{DBt}).
a4. MOSFET of corresponding phase only turns OFF in spite of control input signal level, but there is no Fo signal output.
a5. V_{DB} level reaches UV_{DBr}.
a6. Normal operation : MOSFET ON and outputs current.

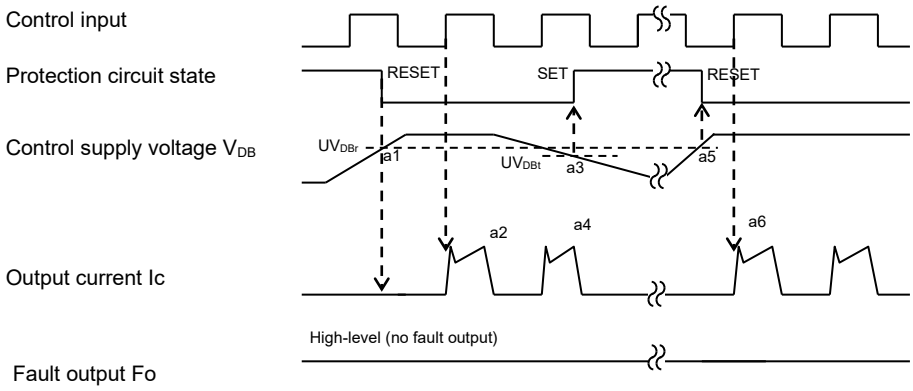


Fig.2-2-5 Timing Chart of P-side UV protection

CHAPTER 3 SYSTEM APPLICATION GUIDANCE

This chapter states special notice for Full SiC DIP application method and design hints (ex: SOA, SCSOA, power life cycles, power loss and thermal dissipation calculation, Noise and ESD withstand capability). For general application method and interface circuit design hints, please refer to Super mini DIPIPM Ver.6 series application note.

3.1 Application Guidance

3.1.1 SOA of DIP Ver.6

The following describes the SOA (Safety Operating Area) of Full SiC DIP.

V_{DSS} : Maximum rating of MOSFET drain-source voltage

V_{DD} : Supply voltage applied on P-N terminals

$V_{DD(surge)}$: Total amount of V_{DD} and surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{DD(PROT)}$: DC-link voltage that DIPIPM can protect itself.

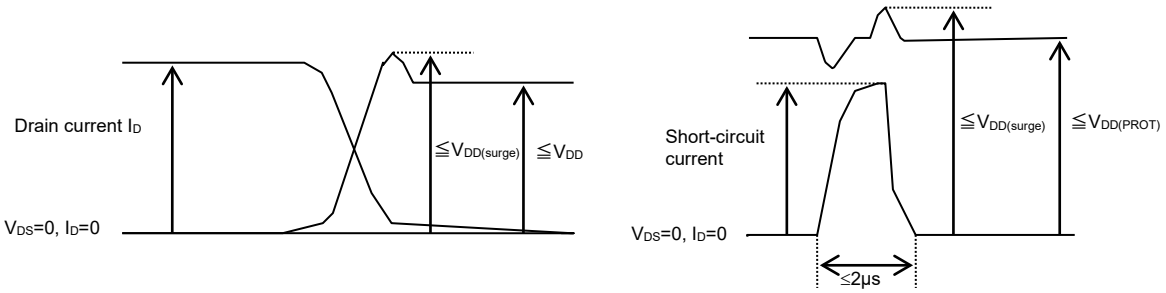


Fig.3-1-1 SOA at switching mode and short-circuit mode

In Case of switching

V_{DSS} represents the maximum voltage rating (600V) of the MOSFET. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{DSS} is $V_{DD(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from $V_{DD(surge)}$ derives V_{DD}, that is 450V.

In Case of Short-circuit

V_{DSS} represents the maximum voltage rating (600V) of the MOSFET. By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{DSS} is $V_{DD(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from $V_{DD(surge)}$ derives V_{DD}, that is, 400V.

3.1.11 SCSOA

Fig.3-1-2 shows the typical SCSOA performance curves of PSF15S92F6-A.

Conditions: V_{DD}=400V, Tch=125°C at initial state, $V_{DD(surge)}$≤500V(surge included), non-repetitive, 2m load

In the case of PSF15S92F6-A, it can shutdown safely an SC current that is about 13 times of its current rating under the conditions only if the MOSFET conducting period is less than 4.0μs. Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

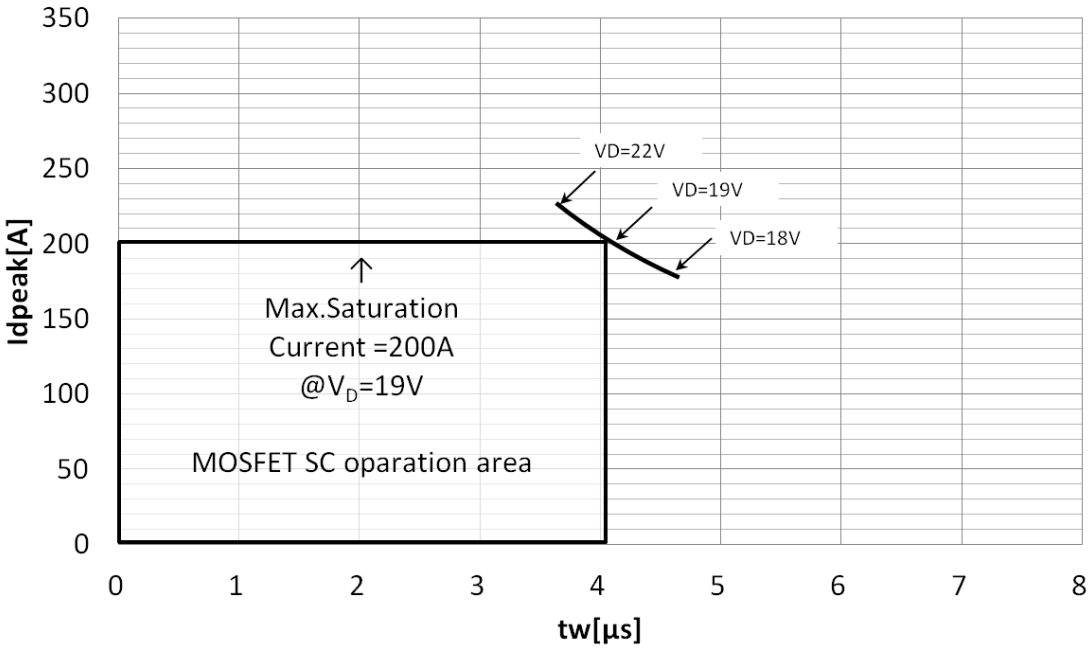


Fig.3-1-2 Typical SCSOA performance curve for PSF15S92F6-A

3.1.12 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happens on the MOSFET channels (ΔTch). The amplitude and the times of the channel temperature variation affect the device lifetime.
Fig.3-1-3 shows the MOSFET power cycle curve as a function of average channel temperature variation (ΔTch).
(The curve is a regression curve based on 3 points of ΔTch=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation.)

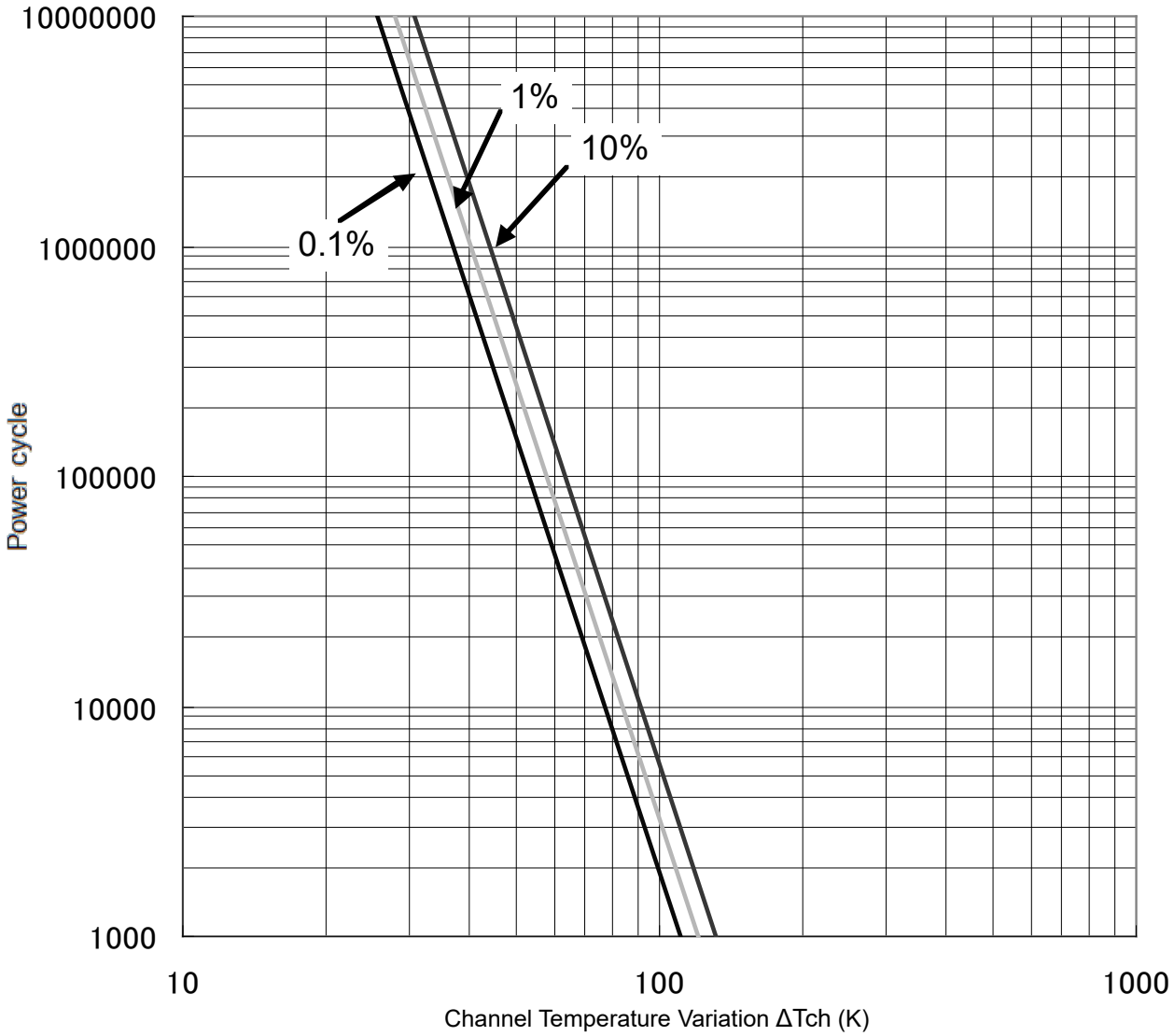


Fig.3-1-3 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.
(6) When turning on the signal (like complementary switching), the channel of the MOSFET conducts by the ON signal and its current path is parallel to the body diode portion and the MOSFET channel portion. (So-called Reverse conduction of MOSFET)

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = I_{DP} \times \sin x$$

$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{DS(on)}$ and $V_{SD(on)}$ at the phase x can be calculated by using a linear approximation:

$$V_{DS(on)} = V_{DS(on)}(@I_{DP} \times \sin x)$$

$$V_{SD(on)} = (-1) \times V_{SD(on)}(@I_{SP}(= I_{DP}) \times \sin x)$$

Thus, the static loss of MOSFET is given by:

$$\frac{1}{2\pi}\int_0^{\pi}(I_{DP} \times \sin x) \times V_{DS(on)}(@I_{DP} \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of MOSFET reverse conduction is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi}((-1) \times I_{DP} \times \sin x)((-1) \times V_{SD(on)}(@I_{DP} \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of MOSFET, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi}(Psw(on)(@I_{DP} \times \sin x) + Psw(off)(@I_{DP} \times \sin x)) \times fc \bullet dx$$

MOSFET recovery characteristics can be approximated by the ideal curve shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

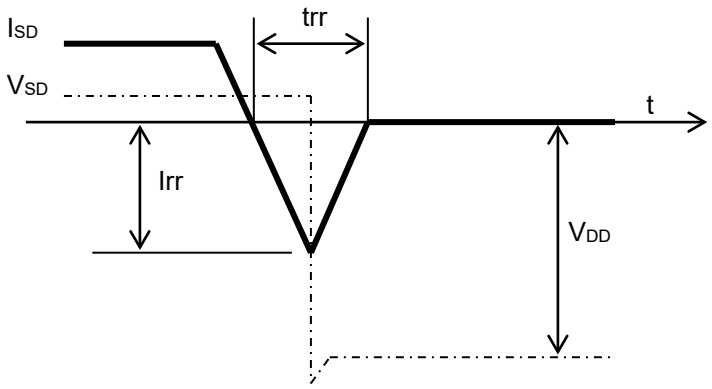


Fig.3-2-1 Ideal MOSFET recovery characteristics curve

$$Psw = \frac{Irr \times V_{DD} \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

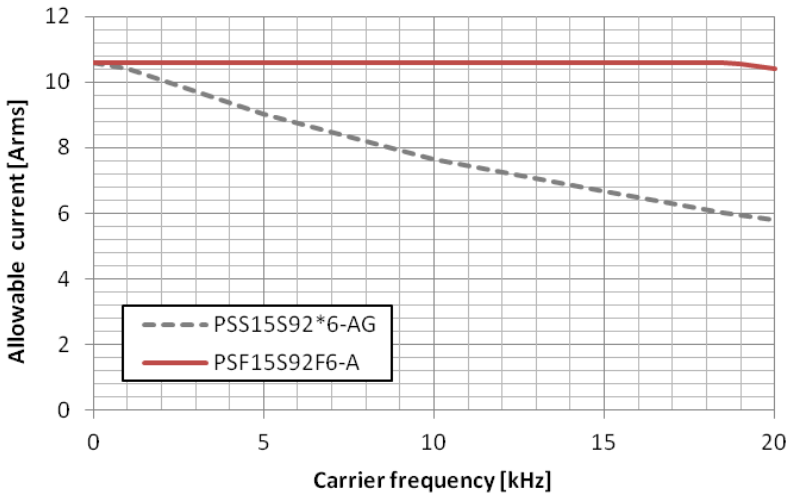
$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@I_{DP} \times \sin x) \times V_{DD} \times trr(@I_{DP} \times \sin x)}{4} \times fc \bullet dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@I_{DP} \times \sin x) \times V_{DD} \times trr(@I_{DP} \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{DS(on)}$, $V_{SD(on)}$, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{DS(on)}$, $V_{SD(on)}$ and Psw(on, off) should be the values at T_{ch}=125°C.

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-2-2 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results. The result is compered with Super mini DIPIPM Ver.6 series (PSS15S92*6-AG) as reference.



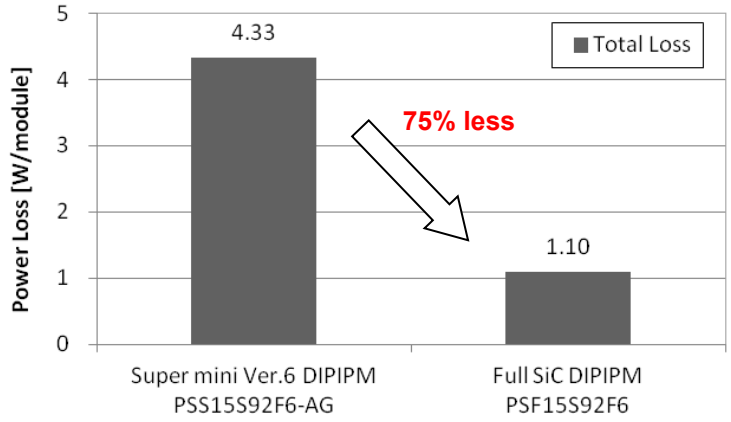
[Common calculation condition]
Simulation model: 3 phase PWM
Vcc=V_{DD}=300V, M=1, P.F=0.8, fo=60Hz,
T_j=T_{ch}=125°C, T_c=100°C, $\Delta T_{(ch-c)}$=25K,
$R_{th(ch-c)}$=Max.

[Calculation condition for PSS15S92F6-AG]
V_D=V_{DB}=15V, V_{CE}=Typ., V_{EC}=Typ.,
Switching loss=Typ.

[Calculation condition for PSF15S92F6-A]
V_D=V_{DB}=18V, $V_{DS(on)}$=Typ., $V_{SD(on)}$=Typ.,
Switching loss=Typ.

Fig.3-2-2 Effective current-carrier frequency characteristics

Fig.3-2-2 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tc=100°C. Tch=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously. Fig.3-2-3 and 3-2-4 are loss simulation results (Typical) compared with PSF15S92F6-A and PSS15S92F6-AG.

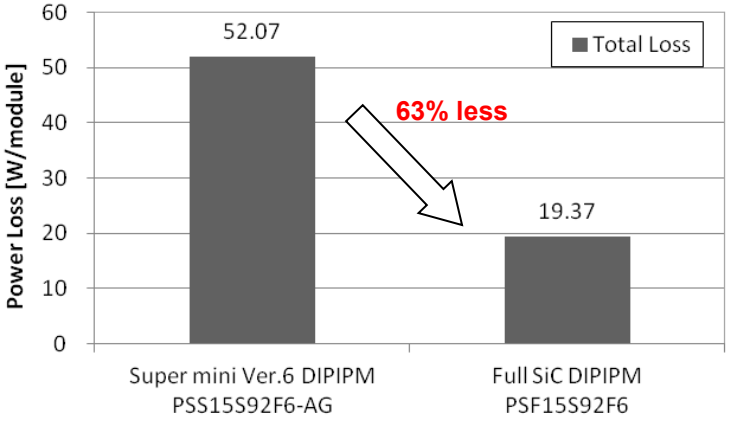


[Common calculation condition]
Simulation model: 3 phase PWM
Vcc=V_{DD}=300V, M=1, P.F=0.8, **Io=1Arms**,
fc=5kHz, fo=60Hz, T_j=T_{ch}=125°C

[Calculation condition for PSS15S92F6]
V_D=V_{DB}=15V, V_{CE}=Typ., V_{EC}=Typ.,
Switching loss=Typ.

[Calculation condition for PSF15S92F6]
V_D=V_{DB}=18V, $V_{DS(on)}$=Typ., $V_{SD(on)}$=Typ.,
Switching loss=Typ.

Fig.3-2-3 Typical loss simulation results



[Common calculation condition]
Simulation model: 3 phase PWM
Vcc=V_{DD}=300V, M=1, P.F=0.8, **Io=7Arms**,
fc=15kHz, fo=60Hz, T_j=T_{ch}=125°C

[Calculation condition for PSS15S92F6]
V_D=V_{DB}=15V, V_{CE}=Typ., V_{EC}=Typ.,
Switching loss=Typ.

[Calculation condition for PSF15S92F6]
V_D=V_{DB}=18V, $V_{DS(on)}$=Typ., $V_{SD(on)}$=Typ.,
Switching loss=Typ.

Fig.3-2-4 Typical loss simulation results

3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

Full SiC DIP have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-3-1. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

Test conditions:

V_{CC}=300V, V_D=18V, Ta=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

Test circuit:

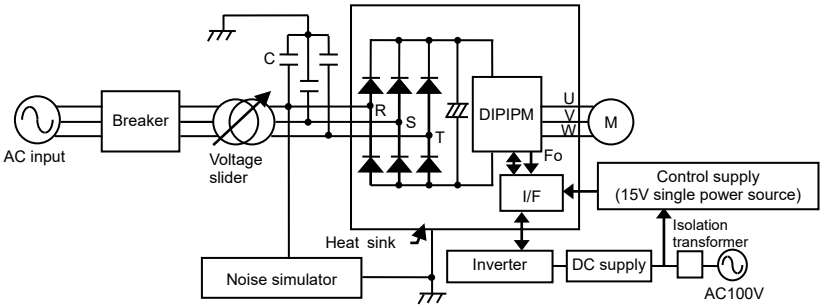


Fig.3-3-1 Noise withstand capability evaluation circuit

C1: AC line common-mode filter 4700pF, 18V single power supply, Test is performed with IM, PWM signals are input from microcomputer by using optocouplers

3.3.2 Countermeasures and Precautions

DIPIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, below countermeasures are recommended.

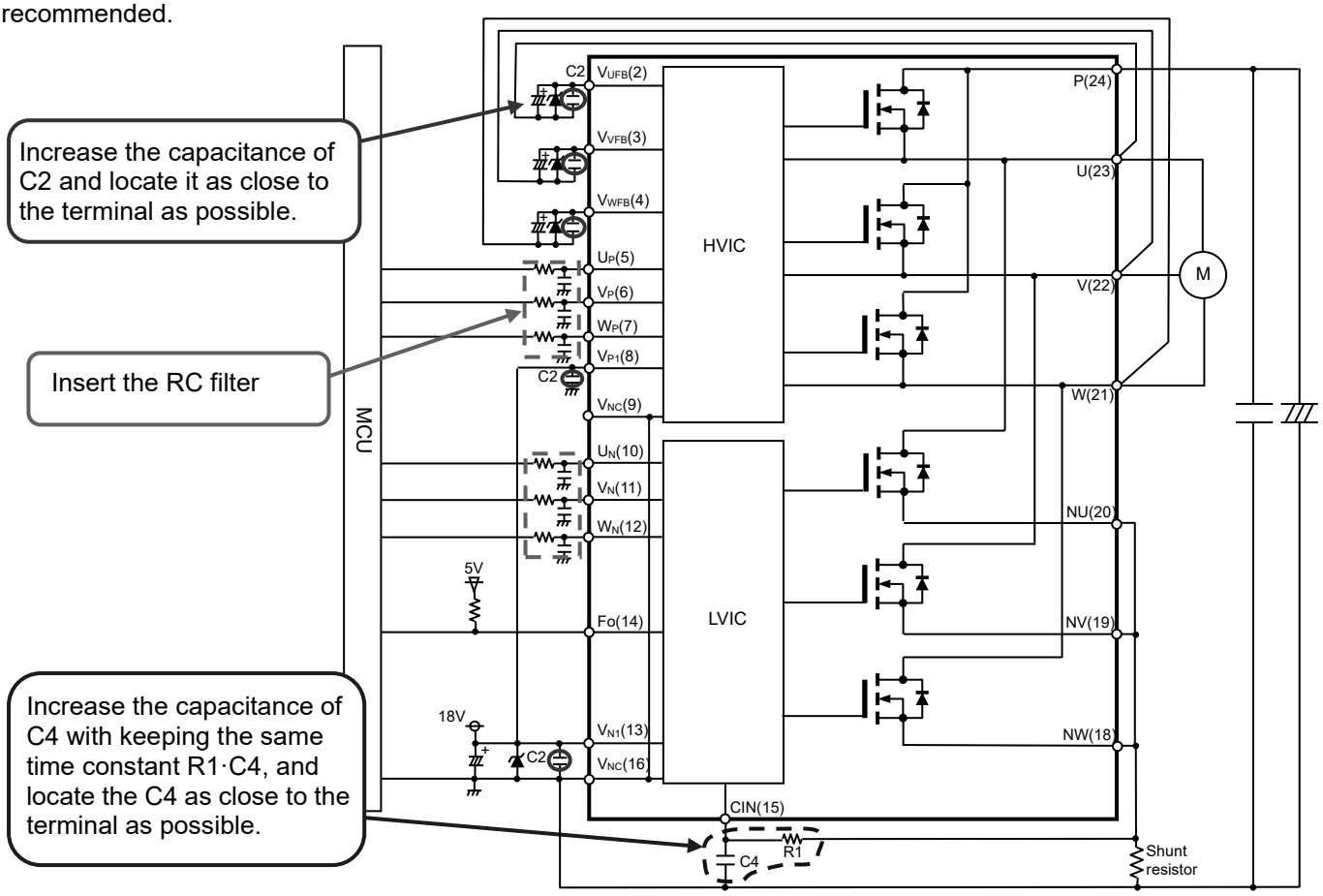


Fig.3-3-2 Example of countermeasures for inverter part

3.3.3 Static Electricity Withstand Capability

Full SiC DIP has been confirmed the change in the V-I characteristics between each terminal and VNC or N terminal before and after applying positive and negative voltage. The test circuit is shown in Fig.3-3-3, 4. Its RC constant is set R=0Ω, C=200pF for MM method, and R=1.5kΩ, C=100pF for HBM method.

For MM method, Full SiC DIP has been confirmed to be with +/-200V or more withstand capability against static electricity. It also has been confirmed to be with +/-1kV or more for HBM method.
For further details, please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor.

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage.
(Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

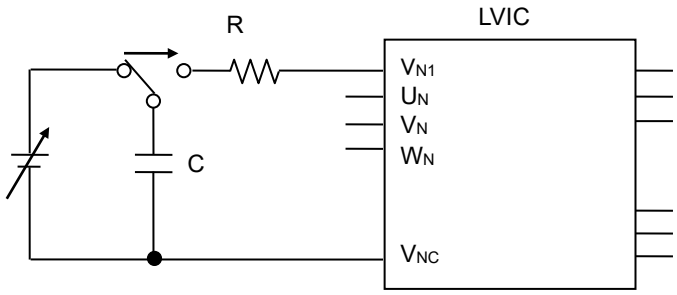


Fig.3-3-3 LVIC terminal Surge Test circuit

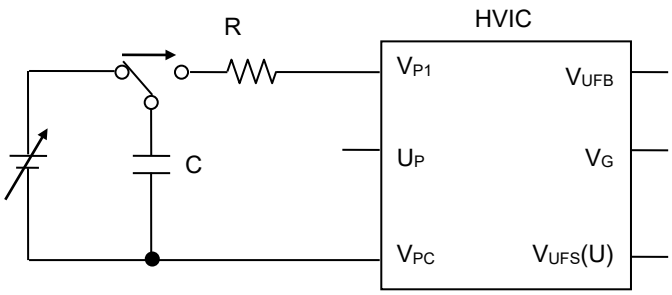


Fig.3-3-4 HVIC terminal Surge Test circuit

CHAPTER 4 Bootstrap Circuit Operation

This chapter states special notice for Full SiC DIP bootstrap circuit characteristics (ex: circuit current at swiching state and diode characteristics). For general bootstrap circuit operation and its design hints, please refer to Super mini DIPIPM Ver.6 series application note and DIPIPM Bootstrap Circuit Design Manual.

4.1 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 0.38mA for PSF15S92F6-A. But at switching state, because gate charge and discharge are repeated by switching, the circuit current exceeds 0.38mA and increases proportional to carrier frequency. For reference, Fig.4-1-1 shows its I_{DB} - carrier frequency fc characteristics.

Conditions: V_D=V_{DB}=18V, V_{DD}=450V, Tch=125°C

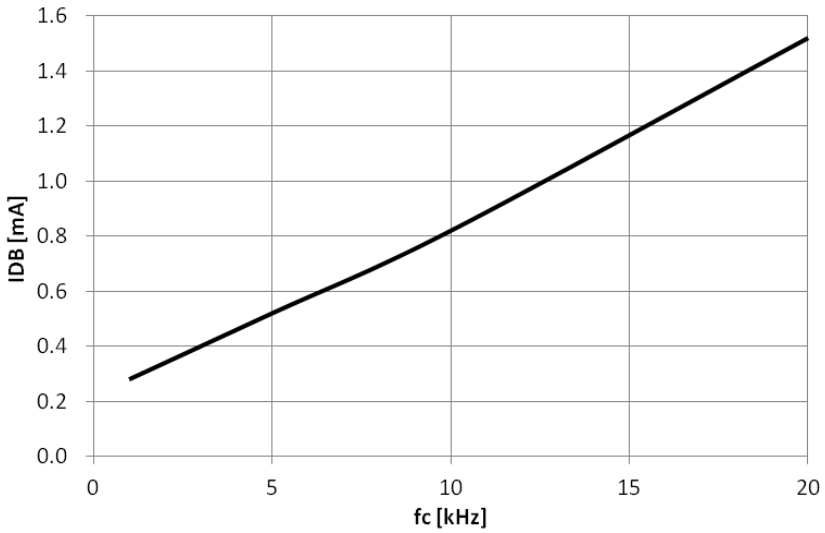


Fig.4-1-1 I_{DB} vs. Carrier frequency for PSF15S92F6-A

4.2 Bootstrap diode

Full SiC DIP integrates bootstrap diode for P-side driving supply. This BSD incorporates current limiting resistor. The VF-IF characteristics (including voltage drop by built-in current limiting resistor) is shown in Fig.4-2-1 and Table 4-2-1.

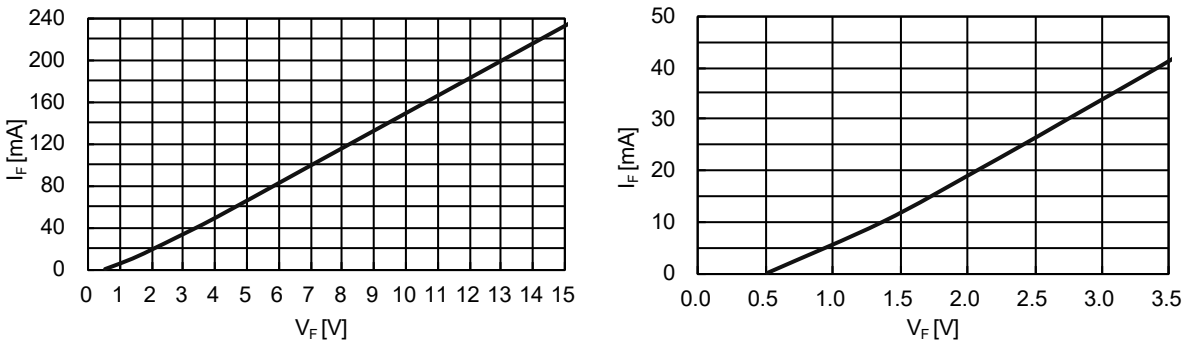


Fig.4-2-1 V_F-I_F curve for bootstrap Diode (the right figure is enlarged view)

Table 4-2-1 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	I_F=10mA including voltage drop by limiting resistor	0.9	1.3	1.7	V
Built-in limiting resistance	R	Included in bootstrap Di	48	60	72	Ω

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